

Fig. 1A

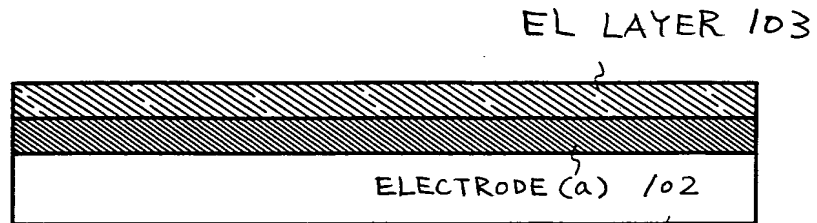


Fig. 1B, PLASMA PROCESSING STEP

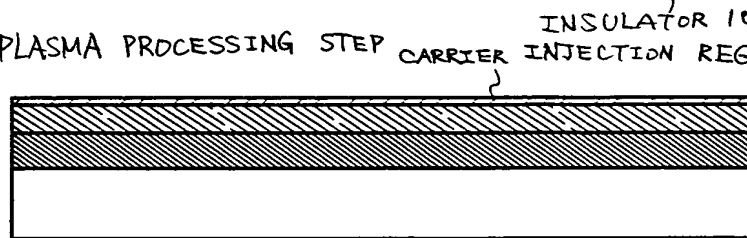


Fig. 1C

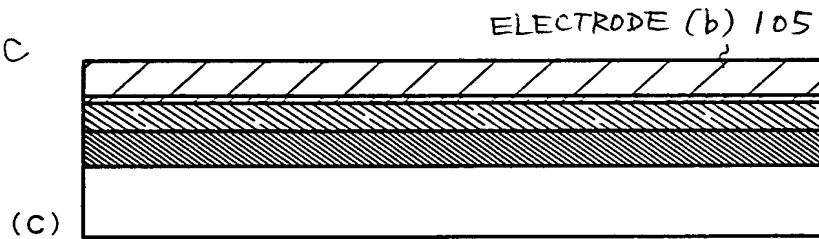
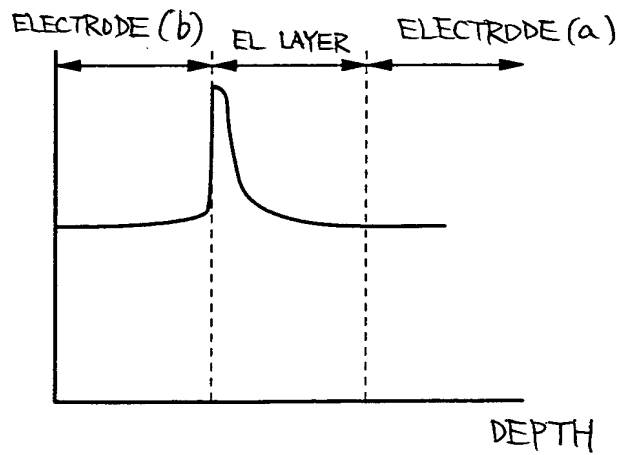
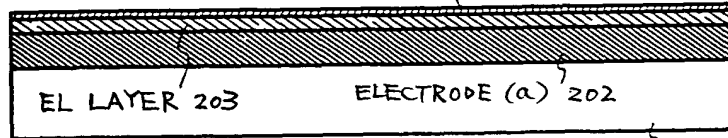


Fig. 1D



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Fig. 2A PLASMA PROCESSING STEP CARRIER BLOCKING REGION (a) 204



INSULATOR 201

Fig. 2B PLASMA PROCESSING STEP CARRIER BLOCKING REGION (b) 205

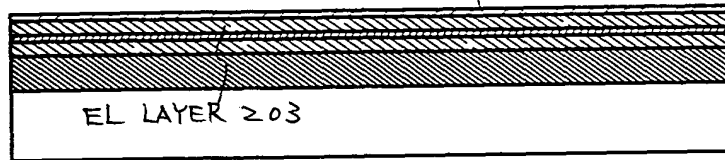


Fig. 2C EL LAYER 203 ELECTRODE (b) 206

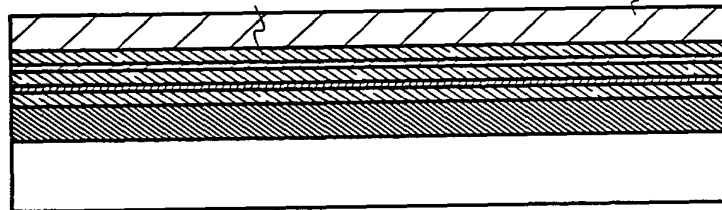


Fig. 3A

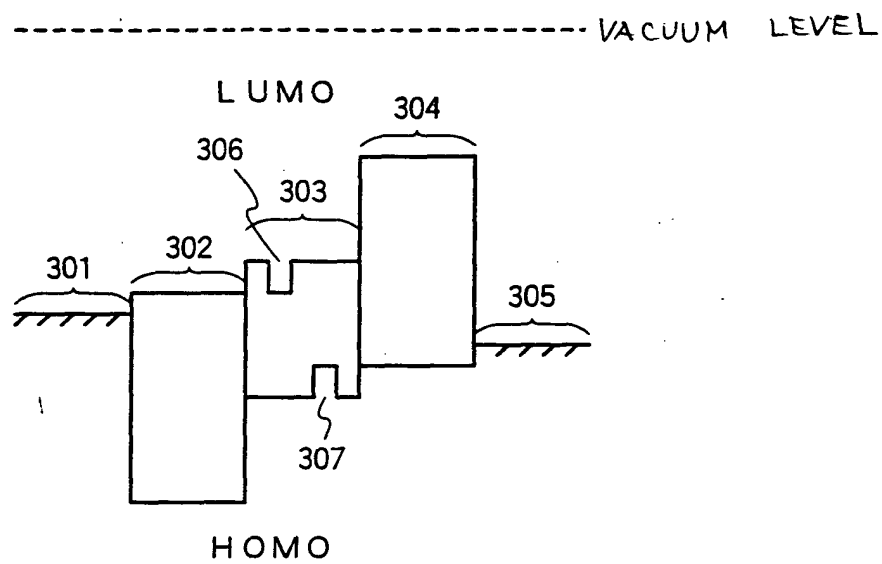


Fig. 3B

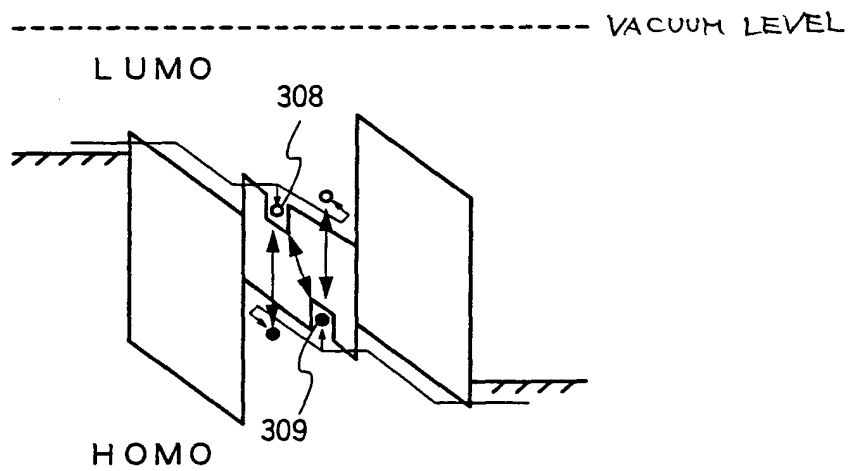


Fig. 4A

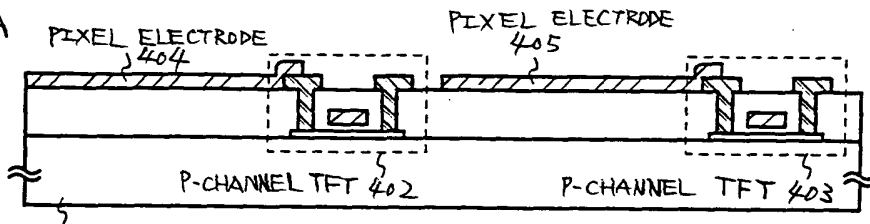


Fig. 4B

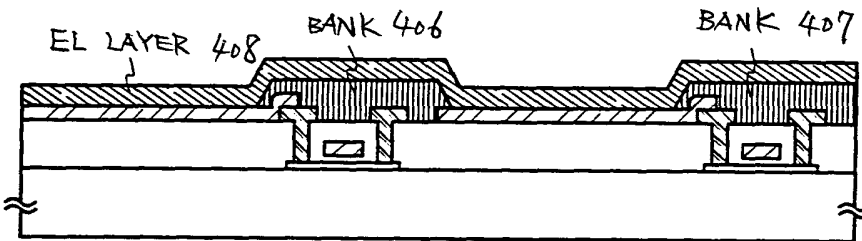


Fig. 4C

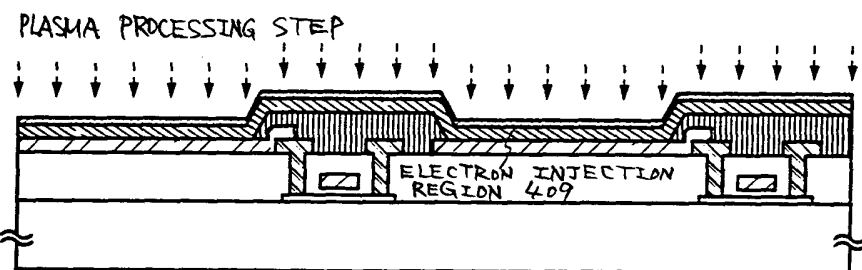
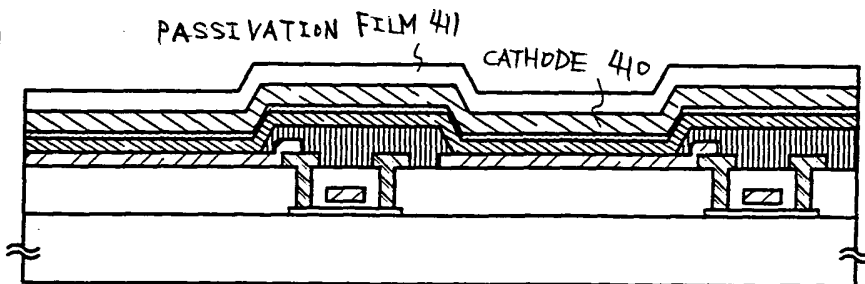


Fig. 4D



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Fig. 5A

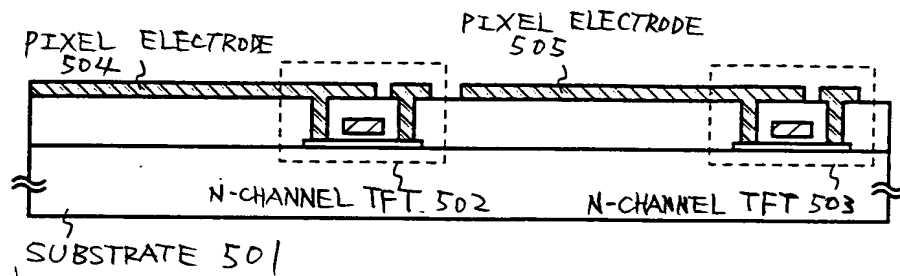


Fig. 5B

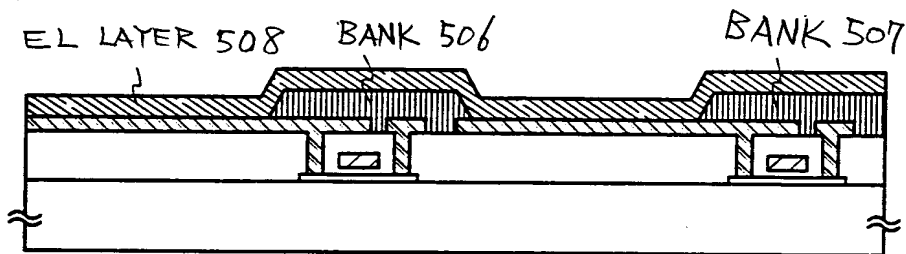


Fig. 5C

PLASMA PROCESSING STEP

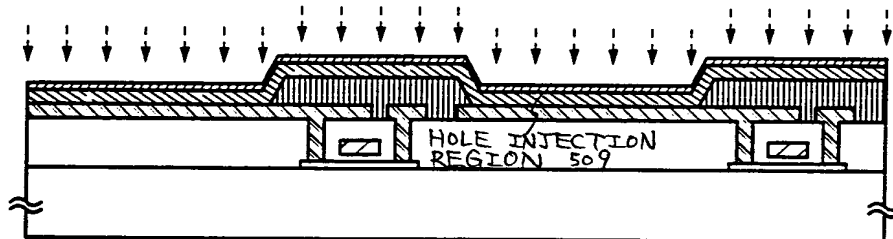


Fig. 5D

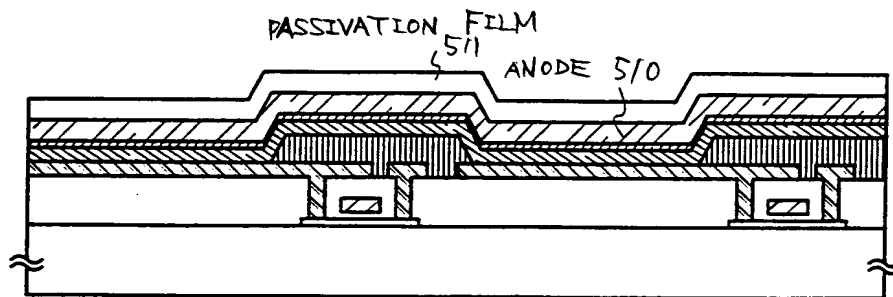


Fig. 6A

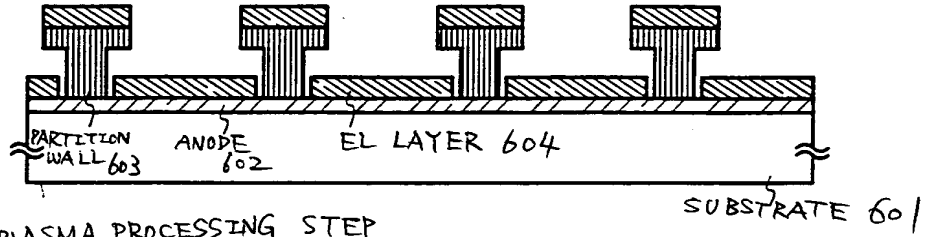


Fig. 6B PLASMA PROCESSING STEP

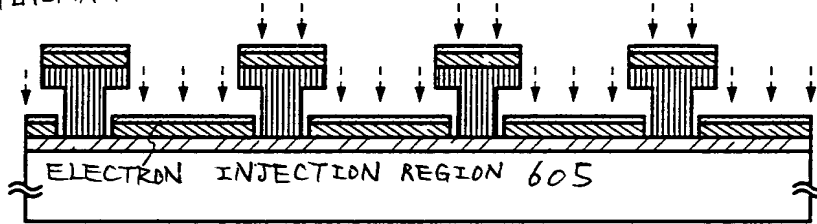
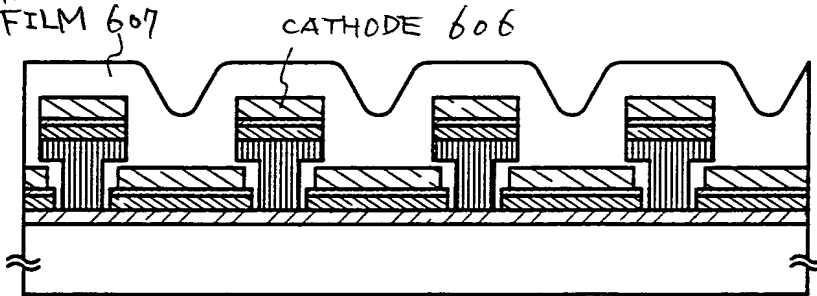


Fig. 6C PASSIVATION FILM 607



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Fig. 7A

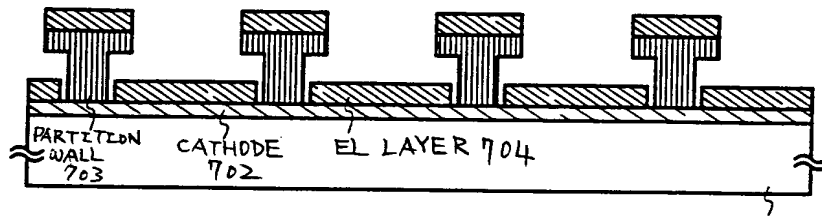


Fig. 7B PLASMA PROCESSING STEP

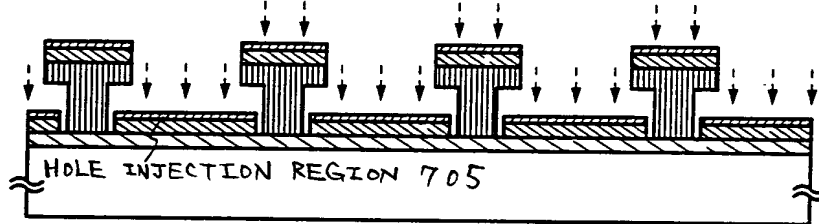
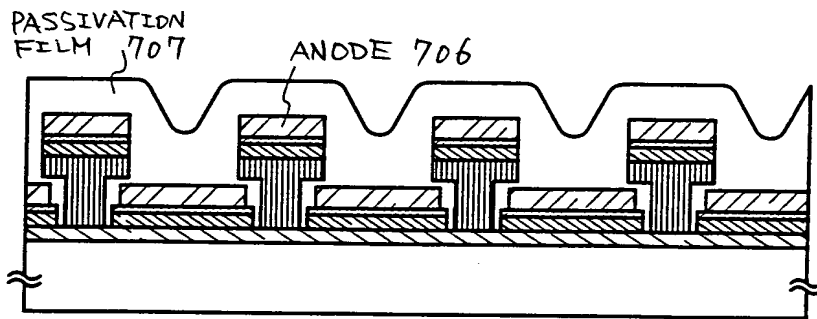


Fig. 7C



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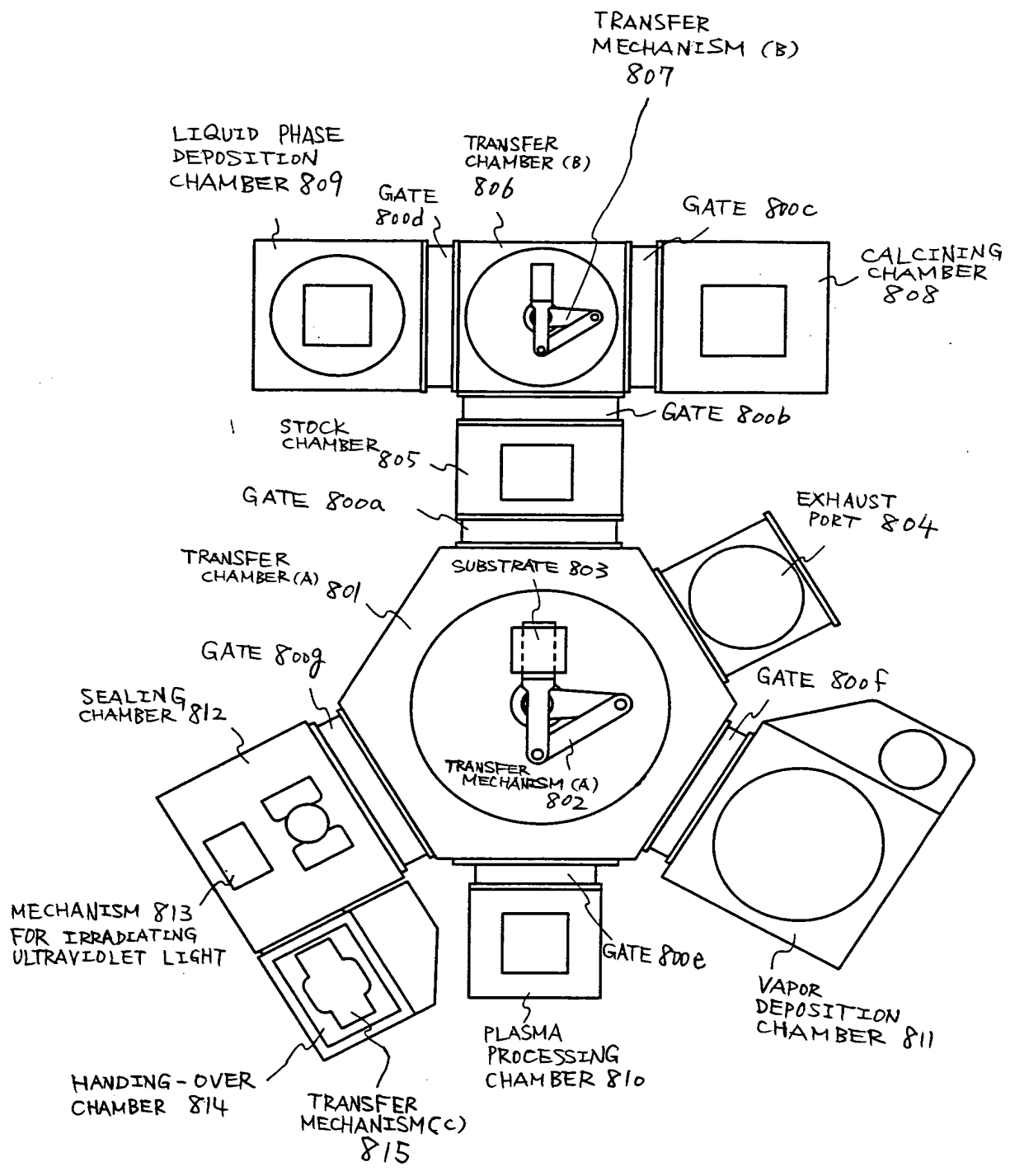
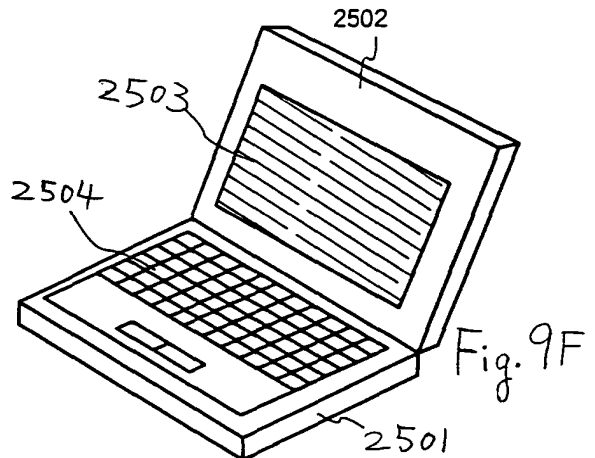
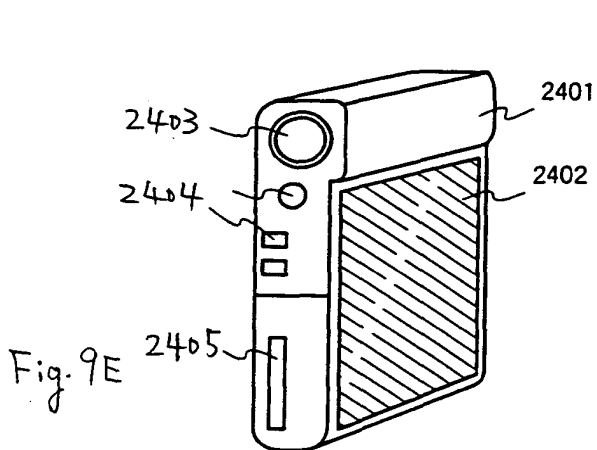
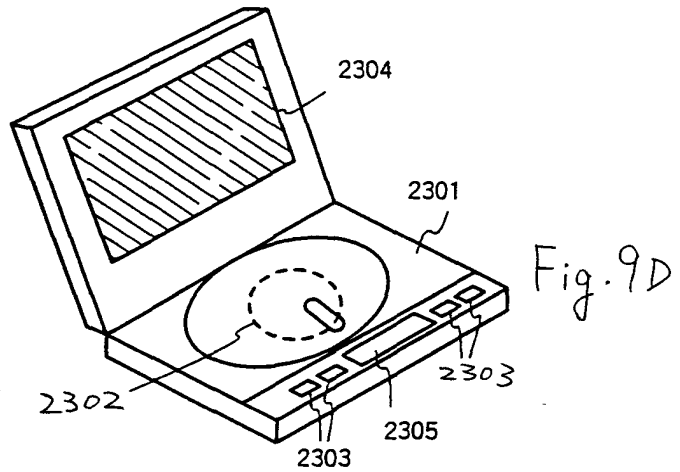
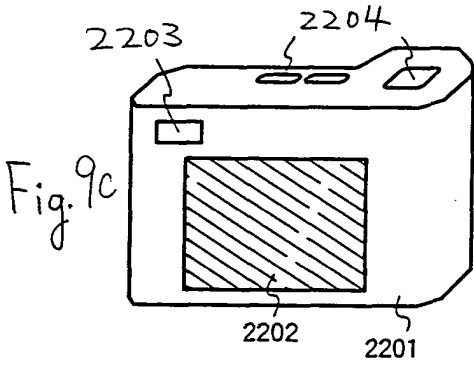
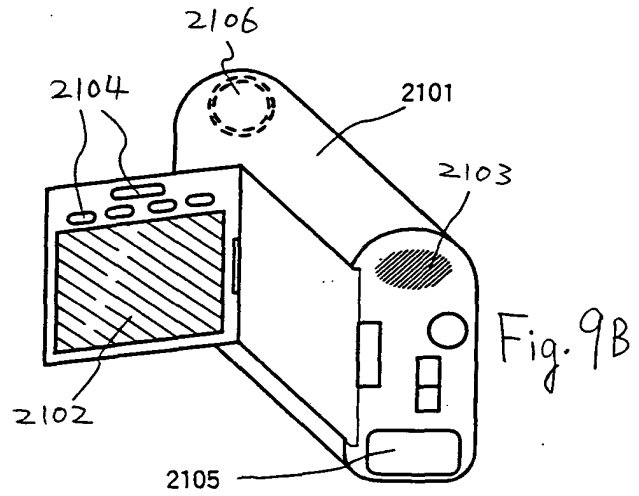
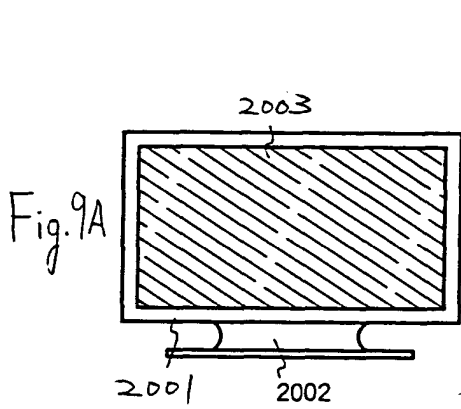


Fig. 8



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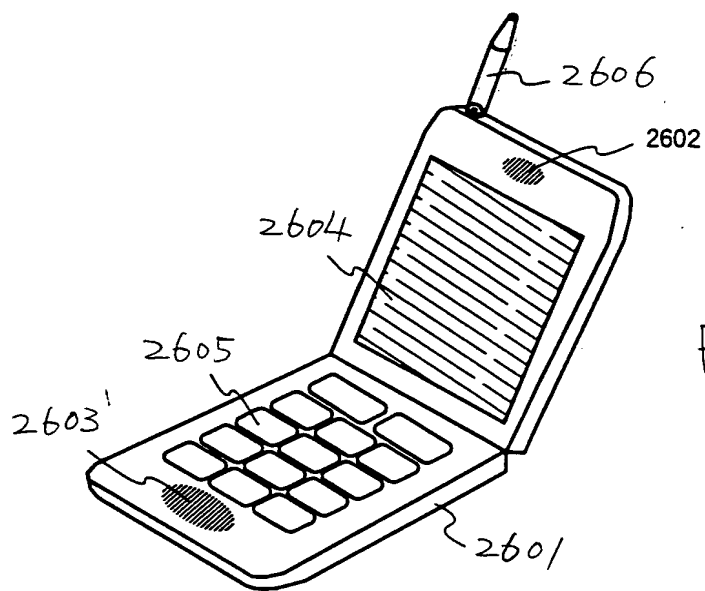


Fig. 10A

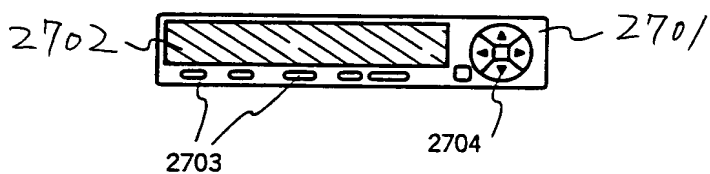


Fig. 10B